

REMARKS

The Examiner's Action mailed on March 28, 2003 has been received and its contents carefully considered.

In this Amendment, claims 1, 4, 5 and 7 have been amended, and claims 9 and 10 have been cancelled. Claims 1, 4, 5 and 7 are the independent claims. Claims 1-8 remain pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

It is noted with appreciation that the Examiner considered the subject matter of claim 9 as being allowable over the art of record. In response thereto, this allowable subject matter has been amended into independent claim 5, thus rendering all of the Examiner's prior art rejections against independent claim 5 and dependent claim 6 moot.

The Examiner has rejected claims 1, 4 and 8 as being anticipated by *Marrs et al.* (USP 5,583,378). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

Applicant's independent claim 1 is directed to a semiconductor device which includes, *inter alia*, a heat spreader having a flat principal surface and having a semiconductor chip and a wiring board provided over the flat principal surface. A common adhesive layer is provided, which is in direct contact with and over the principal surface of the heat spreader and is in direct contact with both the semiconductor chip and the wiring board so as to bond both the semiconductor chip and the wiring board to the heat spreader, so that a heat transfer effect between the semiconductor chip and said heat spreader is about equal to a heat transfer effect between the wiring board and

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the heat spreader. As such, this claimed configuration reduces any adverse effects which may be caused by uneven heat transferring, such as warping or inadvertent separation of the various components from the heat spreader. Further advantages are discussed in Applicant's specification, which includes preventing concave portions and voids from being formed. This claimed device is not disclosed or suggested by the cited reference.

Marrs et al. disclose a ball grid array IC package, which includes a chip 202 that is adhered to a thermal conductor 204 using an adhesive 206. This reference also discloses using an adhesive layer 210 to adhere thermal conductor 204 to substrate 208. Further, this reference teaches that an optional adhesive layer 228 may be provided on the surface of the thermal conductor 204. As shown in Figure 2A, it appears that the adhesive layer 210 and the adhesive 206 are adhered to the thermal conductor 204 using the optional adhesive layer 228.

However, and in contrast to the present invention, this reference does not disclose or suggest a common adhesive layer that is in direct contact with and over a principal surface of the heat spreader and is in direct contact with both the semiconductor chip and the wiring board so as to bond both the semiconductor chip and the wiring board to the heat spreader. The only common adhesive layer disclosed by the cited reference is the optional adhesive layer 228, which as discussed above, is NOT in direct contact with both the chip 202 and the substrate 208, but is instead separated from the chip and substrate by the respective adhesive layers 206 and 210. As such, the configuration disclosed by the cited reference will not enjoy the advantages

that are associated with the invention recited in Applicant's independent claim 1 and dependent claim 8.

Moreover, Applicant's independent claim 4 is submitted to be patentably distinguishable over the cited reference for at least the following reasons. Claim 4 recites a method of manufacturing a semiconductor device, which includes forming a common adhesive layer over a principal surface of a heat spreader, and disposing a semiconductor chip and a wiring board over, and in direct contact with, the common adhesive layer. In contrast, and as noted above, the cited reference discloses separating the common adhesive layer 228 from the chip 202 and the substrate 208 by the respective adhesive layers 206 and 210, so that the adhesive layer 228 is not in direct contact with these features 202 and 208, as would be required by claim 4. As such, the method disclosed by the cited reference will not enjoy the advantages that are associated with the invention recited in Applicant's independent claim 4. It is thus requested that this rejection be withdrawn, and that these claims be allowed.

The Examiner has further rejected claims 2 and 3 as being obvious over *Marrs et al.*, and further in view of *Yamagata et al.* (USP 5,828,127). As noted above, Applicant's independent claim 1 is *prima facie* patentably distinguishable over *Marrs et al.* Moreover, *Yamagata et al.* only disclose providing a fin 19 which is attached utilizing an adhesive 20. This reference does not overcome the above-noted deficiencies of *Marrs et al.*, so that the resulting combination does not disclose or otherwise suggest the features recited within independent claim 1. As such, dependent claims 2 and 3 are submitted to be patentably distinguishable over the cited combination of references for at least the same reasons as independent claim 1, from which these claims depend, as

well as for the additional features recited therein. It is requested that these claims be allowed and it is further requested that these rejections be withdrawn.

The Examiner has rejected claims 5-7 and 10 as being obvious over *Marrs et al.* in view of *Yamagata*, and further in view of *Shin* (USP 5,807,769). It is submitted that these claims are patentably distinguishable over the cited references for at least the following reasons.

As noted above, claim 5 has been amended to include the subject matter of allowable claim 9. Further, claim 6 depends from allowable claim 5, and claim 10 has been cancelled. Thus, this rejection, as it applies to claims 5, 6 and 10, has been rendered moot.

Moreover, claim 7 is submitted to be patentably distinguishable over the cited references for at least the following reasons.

Claim 7 is directed to a method in which, after electrodes are connected to a wiring board by metal thin wires, a second adhesive layer and part of the semiconductor chip are sealed with an encapsulating resin. After the encapsulating resin has only partially cured, the metal thin wires and the semiconductor chip are sealed with more of the encapsulating resin. The advantages of this method are discussed in Applicant's specification. This claimed method is neither disclosed nor suggested by the cited references.

The only reference relied upon by the Examiner that discloses utilizing two resin operations is *Shin*. This reference discloses providing leads 4 around a chip 2, and using a first encapsulating part 6, 6a and a second encapsulating part 7a, 7b, to seal the chip 2 and the leads 4. However, as is clear from the specification of this reference,

the second encapsulating part 7a, 7b is only applied after the first encapsulating part 6, 6a is fully cured. Thus, the method disclosed by *Shin*, even if combined with the teachings of the other cited references, would not enjoy the advantages associated with Applicant's claimed invention. As such, it is submitted that claim 7 is *prima facie* patentably distinguishable over the combination relied upon by the Examiner, and it is requested that this claim be allowed. It is further requested that this rejection be withdrawn.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



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